AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-18. (Cancelled).

19. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding gate line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the gate line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control

window, and further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

20. (Cancelled).

21. (Previously Presented): The liquid crystal display as claimed in claim 19, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

22. (Previously Presented): The liquid crystal display as claimed in claim 19, wherein the interlayer insulation film has a thickness of at least 1 μm.

23. (Previously Presented): The liquid crystal display as claimed in claim 19, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

24. (Previously Presented): The liquid crystal display as claimed in claim 19, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

25. (Previously Presented): The liquid crystal display as claimed in claim 24, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

26. (Previously Presented): The liquid crystal display as claimed in claim 24, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

27. (Previously Presented): The liquid crystal display as claimed in claim 24, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

28. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, and further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

29. (Cancelled).

30. (Previously Presented): The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

31. (Previously Presented): The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness of at least 1 μm.

32. (Previously Presented): The liquid crystal display as claimed in claim 28, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

33. (Previously Presented): The liquid crystal display as claimed in claim 28, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

34. (Previously Presented): The liquid crystal display as claimed in claim 33, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

35. (Previously Presented): The liquid crystal display as claimed in claim 33, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

36. (Previously Presented): The liquid crystal display as claimed in claim 33, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

37. (Currently Amended) A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and a plurality of drain lines formed on the first substrate and defining a plurality of pixels;

a thin film transistor for each pixel formed on the first substrate, the thin film transistor having a gate electrode connected to the corresponding gate line, a drain electrode connected to the corresponding drain line, and a source electrode;

an interlayer insulation film formed over the thin film transistors, the gate lines, and the drain lines;

a pixel electrode for each pixel, the pixel electrode being connected to the source electrode of the corresponding thin film transistor and at least partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding gate line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the gate line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer filled between the first and second substrates; and

a common electrode formed on the second substrate, wherein the common electrode defines an orientation control window disposed across the liquid crystal layer from each pixel, the orientation control window being a region on the second substrate free of the common electrode.

38. (Previously Presented): The liquid crystal display as claimed in claim 37, further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer by an electric field generated by the thin film transistors, the gate lines, and the drain lines.

39. (Previously Presented): The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

40. (Previously Presented): The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness of at least 1 μm.

41. (Previously Presented): The liquid crystal display as claimed in claim 37, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

42. (Previously Presented): The liquid crystal display as claimed in claim 37, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

43. (Previously Presented): The liquid crystal display as claimed in claim 42, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

44. (Previously Presented): The liquid crystal display as claimed in claim 42, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

45. (Previously Presented): The liquid crystal display as claimed in claim 42, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

46. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a column direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

47. (Previously Presented): The liquid crystal display as claimed in claim 46, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

48. (Previously Presented): The liquid crystal display as claimed in claim 46, wherein the interlayer insulation film has a thickness of at least 1 μm.

49. (Previously Presented): The liquid crystal display as claimed in claim 46, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

50. (Previously Presented): The liquid crystal display as claimed in claim 46, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

51. (Previously Presented): The liquid crystal display as claimed in claim 50, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

52. (Previously Presented): The liquid crystal display as claimed in claim 50, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

53. (Previously Presented): The liquid crystal display as claimed in claim 50, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

54. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer from an electric field generated by the thin film transistors, the gate lines, and the drain lines.

55. (Previously Presented): The liquid crystal display as claimed in claim 54, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

56. (Previously Presented): The liquid crystal display as claimed in claim 54, wherein the interlayer insulation film has a thickness of at least 1 μm.

57. (Previously Presented): The liquid crystal display as claimed in claim 54, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

58. (Previously Presented): The liquid crystal display as claimed in claim 54, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

59. (Previously Presented): The liquid crystal display as claimed in claim 58, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

60. (Previously Presented): The liquid crystal display as claimed in claim 54, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

61. (Previously Presented): The liquid crystal display as claimed in claim 54, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

62. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and a plurality of drain lines formed on the first substrate and defining a plurality of pixels;

a thin film transistor for each pixel formed on the first substrate, the thin film transistor having a gate electrode connected to the corresponding gate line, a drain electrode connected to the corresponding drain line, and a source electrode;

an interlayer insulation film formed over the thin film transistors, the gate lines, and the drain lines;

a pixel electrode for each pixel, the pixel electrode being connected to the source electrode of the corresponding thin film transistor and at least partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a column direction ~~and has a~~ and a surface of the pixel electrode which overlaps the gate line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer filled between the first and second substrates; and

a common electrode formed on the second substrate, wherein the common electrode defines an orientation control window disposed across the liquid crystal layer from each pixel, the orientation control window being a region on the second substrate free of the common electrode.

63. (Previously Presented): The liquid crystal display as claimed in claim 62, further comprising means for providing the interlayer insulation film with a thickness sufficient to alleviate an influence on the liquid crystal layer by an electric field generated by the thin film transistors, the gate lines, and the drain lines.

64. (Previously Presented): The liquid crystal display as claimed in claim 62, wherein the interlayer insulation film has a thickness of at least 0.5 μm.

65. (Previously Presented): The liquid crystal display as claimed in claim 62, wherein the interlayer insulation film has a thickness of at least 1 μm.

66. (Previously Presented): The liquid crystal display as claimed in claim 62, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

67. (Previously Presented): The liquid crystal display as claimed in claim 62, wherein at least a part of each thin film transistor and/or gate line and/or drain line is disposed beneath a corresponding pixel electrode.

68. (Previously Presented): The liquid crystal display as claimed in claim 67, wherein the interlayer insulation film has a thickness which is equal to or greater than half of an interval between two adjacent pixel electrodes.

69. (Previously Presented): The liquid crystal display as claimed in claim 67, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than twice the thickness of the interlayer insulation film.

70. (Previously Presented): The liquid crystal display as claimed in claim 67, wherein the width by which a part of each thin film transistor and/or gate line and/or drain line is projected from under a corresponding pixel electrode is no more than half of an interval between two adjacent pixel electrodes.

71. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the

pixel electrode is overlapped with the corresponding gate line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the gate line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and the interlayer insulation film has a thickness of at least 1μm.

72. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, wherein the interlayer insulation film has a thickness of at least 1μm.

73. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and a plurality of drain lines formed on the first substrate and defining a plurality of pixels;

a thin film transistor for each pixel formed on the first substrate, the thin film transistor having a gate electrode connected to the corresponding gate line, a drain electrode connected to the corresponding drain line, and a source electrode;

an interlayer insulation film formed over the thin film transistors, the gate lines, and the drain lines, and having a thickness of at least 1μm;

a pixel electrode for each pixel, the pixel electrode being connected to the source electrode of the corresponding thin film transistor and at least partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding gate line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the gate line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer filled between the first and second substrates; and

a common electrode formed on the second substrate, wherein the common electrode defines an orientation control window disposed across the liquid crystal layer from each pixel, the orientation control window being a region on the second substrate free of the common electrode.

74. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a column direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation control window created in the common electrode; wherein

orientation direction of liquid crystal is divided by weak electric fields and/or electric fields in a sloped direction generated by the orientation control window, and the interlayer insulation film has a thickness of at least 1μm.

75. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and drain lines formed on the first substrate;

thin film transistors each arranged at an intersection between a corresponding gate line and a corresponding drain line, and having a gate connected

to the corresponding gate line, a drain connected to the corresponding drain line, and a source;

an interlayer insulation film formed covering the thin film transistors, the gate lines, and the drain lines;

a plurality of pixel electrodes each connected to the source of the corresponding thin film transistor and partially formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a row direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposing the first substrate;

a liquid crystal layer arranged between the first and second substrates;

a common electrode formed on the second substrate; and

an orientation dividing portion for dividing an orientation direction of liquid crystal by generating weak electric fields and/or electric fields in a sloped direction, wherein the interlayer insulation film has a thickness of at least 1μm.

76. (Currently Amended): A liquid crystal display, comprising:

a first substrate;

a plurality of gate lines and a plurality of drain lines formed on the first substrate and defining a plurality of pixels;

a thin film transistor for each pixel formed on the first substrate, the thin film transistor having a gate electrode connected to the corresponding gate line, a drain electrode connected to the corresponding drain line, and a source electrode;

an interlayer insulation film formed over the thin film transistors, the gate lines, and the drain lines, and having a thickness of at least 1μm;

a pixel electrode for each pixel, the pixel electrode being connected to the source electrode of the corresponding thin film transistor and at least partially

formed on the interlayer insulation film, wherein the pixel electrode is overlapped with the corresponding drain line extending in a column direction ~~and has a~~ and a surface of the pixel electrode which overlaps the drain line is substantially flat ~~surface~~;

a second substrate disposed opposite the first substrate;

a liquid crystal layer filled between the first and second substrates; and

a common electrode formed on the second substrate, wherein the common electrode defines an orientation control window disposed across the liquid crystal layer from each pixel, the orientation control window being a region on the second substrate free of the common electrode.